

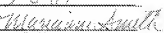
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Jong Shik Yoon, et al.	Docket No.:	TI-37043
Serial No: 10/825,343	Filed:	04/15/2004
Art Unit: 2813	Examiner:	Thanh T. Nguyen
Customer No.: 23494	Conf. No.:	8658
Title:	Minimizing Transistor Variations Due to Shallow Trench Isolation Stress	

ELECTION


Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(A)	
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as first Class Mail in an envelope addressed to Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.	
3-8-07	
Date	
Marianna Smith	

Dear Sir:

With respect to the Restriction Requirement mailed on February 13, 2007, the Examiner required restriction between Species I and Species II. Applicant hereby elects Species I without traverse. Claims 1, 6, and 7 are readable thereon.

Respectfully submitted,


Jacqueline J. Garner
Attorney for Applicant
Reg. No. 36,144

Texas Instruments Incorporated
P.O. Box 855474, M/S 3999
Dallas, TX 75265
(214) 532-9348 or
(972) 917-5643
Fax: (972) 917-4418